Date:

To _____ Document No. DB70211-0E

Transition from PCD46x1 to PCD46x1A

Nippon Pulse Motor, Co., Ltd

Thank you for using our PCD46x1 series.

We would like to inform you the precautions in the transition from PCD46x1 to PCD46x1A.

1. Outline

PCD46x1 has a circuit following bug: A motor may not start when a start command is written after writing a stop command.

The above bug had been corrected in PCD46x1A. However, for correction, procedures to write and read were slightly changed.

PCD46x1A's package and terminal allocation are the same as PCD46x1's. PCD46x1A can be mounted on the board for PCD46x1.

2. Difference of procedure to write to / read out register

When $\overline{WRQ}$ output is used, $\overline{WRQ}$ output signal width changes and the following procedure difference is processed automatically

2-1. Procedure to write to register

Procedure	PCD46x1	PCD46x1A
1	Write a Register selection command to COMBF.	Same as left.
2	Write the upper data to the RegWBF (bits 23 ~16)	Same as left.
3	Write the middle data to the RegWBF (bits 15~8)	Same as left.
4	Write the lower data to the RegWBF (bits 7~0)	Same as left.
5	Wait longer than internal processing time (CLK 2 cycles) when the $\overline{WRQ}$ is not used.	Wait longer than internal processing time (CLK 3 cycles) when the $\overline{WRQ}$ is not used.

2-2. Procedure to read out register

Procedure	PCD46x1	PCD46x1A
1	Write a Register selection command to COMBF.	Same as left
2	Wait longer than internal processing time (CLK 2 cycles) when the $\overline{WRQ}$ is not used.	Wait longer than internal processing time (CLK 3 cycles) when the $\overline{WRQ}$ is not used.
3	Read the data from the RegRBF. The order to read is arbitrary.	Same as left

2-3. Procedure to write start mode command, control command and output mode command

Procedure	PCD46x1	PCD46x1A
1	Write a command to COMBF	Same as left.
2	PCD46x1 internal status changes after internal processing time (CLK 1 cycle).	PCD46x1A internal status changes after internal processing time (CLK 2 cycle).

Note: Only start command among start mode commands follows 2-4. Procedures to write start command.

2-4. Procedure to write start command

Procedure	PCD46x1	PCD46x1A
1	Write a dummy command to COMBF.	**Omitted**
2	Wait longer than internal processing time (CLK 1 cycle) when the $\overline{WRQ}$ is not used.	**Omitted**
3	Write a start command to COMBF.	Same as left.

Note: A dammy command is a command that only the bit 4 of the start command to be used is changed to “0”. It is no problem to perform PCD46x1 procedure with using PCD46x1A.

3. Other differences

3-1. Software

We changed the procedure that $\overline{STP}$ signal or $\overline{EL}$ signal of operation direction is input before $\overline{STA}$ signal is input after a Hold start command is written in PCD46x1 mode (OCM5=1 and RENV.46MD=1).

Item	PCD46x1	PCD46x1A
$\overline{INT}$ output	Does not output	**Outputs**
Subsequent writing start command	Disabled only first time	**Always enabled**

Note: There is no change in other than PCD46x1 mode of PCD46x1A (OCM5=0 or REMV.46MD=0). This operation is the same as PCD46x1. In PCD46x1, the above operation occurs even in other than PCD46x1 mode.

3-2. Hardware

1. PCD46x1A’s package, terminal allocation, absolute maximum rating and recommended operation conditions are the same as PCD46x1’s.
2. Consumption current of DC characteristics slightly increased.

CLK	Model	Consumption current
4.9152MHz	PCD4611	3 mA(Max)
	PCD4621	5 mA(Max)
	PCD4641	9 mA(Max)
10.000MHz	PCD4611	5 mA(Max)
	PCD4621	9 mA(Max)
	PCD4641	17 mA(Max)

Model	Consumption current
PCD4611A	3 mA(Max)
PCD4621A	5 mA(Max)
PCD4641A	**10 mA**(Max)
PCD4611A	**6 mA**(Max)
PCD4621A	**10 mA**(Max)
PCD4641A	**20 mA**(Max)

3. AC characteristics

《Read cycle》

Item	PCD46x1	PCD4611A	PCD4621A	PCD4641A
Address set up time	0 ns (Min)	0 ns (Min)	0 ns (Min)	0 ns (Min)
Address hold time	0 ns (Min)	0 ns (Min)	0 ns (Min)	0 ns (Min)
RD signal width	34 ns (Min)	**29 ns** (Min)	**28 ns** (Min)	**32 ns** (Min)
$\overline{WRQ}$ output delay time	28 ns (Max)	**29 ns** (Max)	**31 ns** (Max)	**32 ns** (Max)
Data output delay time	34 ns(Max)	**29 ns** (Max)	**31 ns** (Max)	**32 ns** (Max)
Data float delay time	18 ns(Max)	**22 ns** (Max)	**22 ns** (Max)	**22 ns** (Max)

《Write cycle》

Item	PCD46x1	PCD4611A	PCD4621A	PCD4641A
Address set up time	0 ns (Min)	0 ns (Min)	0 ns (Min)	0 ns (Min)
Address hold time	0 ns (Min)	0 ns (Min)	0 ns (Min)	0 ns (Min)
WR signal width	14 ns (Min)	**16 ns (Min)**	**17 ns (Min)**	**16 ns (Min)**
$\overline{WRQ}$ delay time	28 ns (Max)	**13 ns (Max)**	**17 ns (Max)**	**16 ns (Max)**
Data set up time	14 ns (Min)	**13 ns (Min)**	14 ns (Min)	**13 ns (Min)**
Data hold time	0 ns (Min)	0 ns (Min)	0 ns (Min)	0 ns (Min)

4. Outline of additional functions

The following PCD46x1A functions are added. Please see “PCD4611A/4621A/4641A User’s Manual” in detail.

1. You can connect CPU with 4-wire serial I/F as well as 8-bit parallel bus I/F connection.
2. When connecting with 4-wire serial I/F, you can use terminals D0~D5 as general-purpose Input/output ports.